

REMARKS**AMENDMENTS**

Claims 8 and 9 has been cancelled. Claim 16, the only independent claim remaining in the application, has been amended to recite the steps for forming the wiring film. Support for this amendment is found in original claims 8 and 9 and in the specification on page 8, lines 16-27. Support for the amendment to claim 11 is found on page 8, lines 16-27. Support for the amendment to claim 17 is found in original claims 8 and 9. Claims 5 and 12 have been amended to more particularly point out and distinctly claim the subject matter that applicant regards as the invention.

Support for newly presented claims 18, 19 and 21 is found on page 8, lines 19-24. Support for newly presented claim 20 is found in original claims 5, 7, 12, and 13.

It is submitted that no new matter is introduced by these amendments and new claims.

OBJECTION TO THE SPECIFICATION

The Title was objected to. The Title was amended by a Supplemental Preliminary Amendment mailed December 4, 2002, to read " A METHOD FOR FORMING A SEMICONDUCTOR DEVICE." It is submitted that this objection has been overcome.

FEATURE OF THE INVENTION AS RECITED IN AMENDED CLAIM 16

The feature of the present invention, as recited in amended independent claim 16, is that after forming the TiN film, which is the base layer of a metal wiring film, the TiN is heat-treated (for example, in a temperature range of 200 to 650°C) before forming the aluminum film, which is the upper layer. This makes the stress direction an extensional direction. As described in the specification "a TiN film is formed as a bottom-layer film 5b of a wiring film through the sputtering method to heat-treat the TiN film in a temperature range of 200 to 650°C." Specification, page 8, lines 16-18. When the TiN film, which immediately after sputtering has a compression-directional stress, is heat-treated, for example, in a temperature range of 200 to 650°C, the stress direction changes to an extensional direction. Therefore, the film has a stress in a direction in which the ferroelectric capacitor characteristics are not deteriorated.

FIRST REJECTION UNDER 35 USC 102

Claims 8, 11, 16, and 17 were rejected under 35 USC 102(b) as anticipated by Arita, U.S. Patent 5,624,864 ("Arita").

As amended, claim 16, the only independent claim remaining in the application recites forming a metal wiring pattern over the second insulating film by the steps of:

- f2a) depositing a TiN layer;
- f2b) heat-treating said TiN layer to create a tensile stress; and
- f2c) depositing an upper layer on said TiN layer.

Arita discloses a semiconductor device having a capacitor and a manufacturing method thereof. Arita, Title. In Figure 7, an insulating layer **46** and a passivation layer **47** composed of silicon nitride are formed. Arita, column 7, lines 22-30. Charge characteristics of the capacitor **41** were measured after heating for 7 minutes at 380°C after forming passivation layer **47**. Arita, column 8, lines 32-41.

However, claim 16 recites the steps of depositing an upper layer on said TiN layer (step f2c) and forming a surface protective film over said second insulating film and said metal wiring pattern (step f3). Arita discloses formation of a second passivation layer **48** made of silicon nitride on passivation layer **47**. Arita, column 8, lines 21-27. However, Arita does not disclose formation of two layers over the TiN layer.

It is axiomatic that for a prior art reference to anticipate under § 102 it has to meet every element of the claimed invention. . . ." *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1980) (emphasis added). Arita does not disclose formation of two layers over the TiN layer. The rejection of claims as anticipated by Arita should be withdrawn.

Further, the person of ordinary skill in the art, having the advantage of the teachings of Arita, would not be motivated to incorporate the heating step disclosed by Arita into another process. Figure 11 shows the leakage current for capacitor **41** for different processing conditions. B shows the value after formation of passivation layer **47**. C shows the value after heating for 7 minutes at 380°C in a mixed gas atmosphere of nitrogen and hydrogen after forming the passivation layer. Arita, column 8, lines 37-41. As shown in Figure 11, and discussed in the specification at column 8, lines 49-65,

leakage current either increases or remains unchanged after heat treatment. This would not motivate the person of ordinary skill in the art to incorporate a heat treatment step into another process.

SECOND REJECTION UNDER 35 USC 102

Claims 5, 8, 9, 11, 16, and 17 were rejected under 35 USC 102(b) as anticipated by Patel, U.S. Patent 5,374,578.

Patel teaches:

Next, a metal interconnect **26** is established by sputter deposition, for example, over glass **18** and in contact windows (**20, 22, 24**), as shown in FIG. **9**. Interconnect **26** can comprise a TiN barrier plus an Al-Si metal, such as aluminum doped with a 1% Si for example. The Al-Si metal can be sputter deposited over the underlying sputtered TiN barrier. The barrier prevents the Al-Si metal from interdiffusing with the top and bottom electrodes during subsequent anneals. The thickness of the TiN barrier is approximately 500Å (50 nm), and the thickness of the Al-Si metal is between 5,000Å (500 nm) and 8,000Å (800 nm).

A fourth photoresist pattern is then established by conventional means over metal interconnect **26**. The exposed metal interconnect layer is then etched, and the fourth photoresist pattern is removed to yield the structure of FIG. **10**.

A fifth anneal in ozone and/or oxygen is then performed. The fifth anneal is done by furnace annealing or RTA. Preferably, a furnace anneal is done at a temperature of less than 450°C. and for no more than 30 minutes.

Patel, column 5, lines 47-68 (emphasis added).

As is apparent from this passage, the heat-treating step ("fifth anneal") is carried out after both the TiN layer and Al-Si layer have been deposited. The heat-treating step is carried out after formation of the fourth photoresist pattern. The fourth photoresist pattern is formed over metal interconnect **26**, which comprises the TiN layer and the Al-Si layer.

In the method recited in the claims, heat treating is carried out after deposition of

the TiN layer and before deposition of the upper layer on the TiN layer. Patel does not disclose heat treating after deposition of the TiN layer and before deposition of the upper layer on the TiN layer. The rejection of claims as anticipated by Patel should be withdrawn.

Further, nothing in Patel would motivate the person of ordinary skill in the art to modify Patel's method to produce the claimed invention. As discussed in the specification, heat treating after deposition of the TiN layer and before deposition of the upper layer changes the direction of the stress in the TiN layer from a compression-directional stress to an extension direction. Specification, page 8, lines 16-24. Patel does not consider stress and, thus, teaches nothing about stress after formation of the TiN layer. Thus, the person of ordinary skill in the art would have no motivation to modify stress by heat treatment.

FIRST REJECTION UNDER 35 USC 103

Claim 12 was rejected under 35 USC 103(a) as unpatentable over Arita in view of Wolfe, Silicon Processing for the VLSI Era, Vol. 1, p. 367 (1986) ("Wolfe, p. 367").

As discussed above, Arita does not disclose formation of two layers over the TiN layer. This deficiency is not overcome by Wolfe, p. 367, which discloses deposition of alloy films and wafer heating while sputtering. Therefore, the rejection of claim 12 as unpatentable over Arita in view of Wolfe, p. 367, should be withdrawn. In addition, claim 12 is indirectly dependent on claim 16 and is allowable as a claim dependent on an allowable claim.

SECOND REJECTION UNDER 35 USC 103

Claim 14 was rejected under 35 USC 103(a) as unpatentable over Arita in view of Wolfe, p. 192.

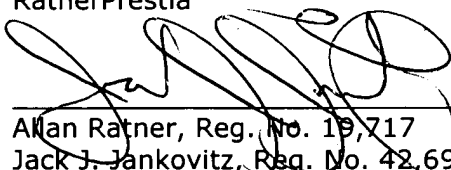
As discussed above, Arita does not disclose formation of two layers over the TiN layer. This deficiency is not overcome by Wolfe, p. 192, which discloses techniques for depositing silicon nitride. Therefore, the rejection of claim 14 as unpatentable over Arita in view of Wolfe, p. 192, should be withdrawn. In addition, claim 14 is directly dependent on claim 16 and is allowable as a claim dependent on an allowable claim.

CONCLUSION

It is respectfully submitted that the claims are in condition for immediate allowance and a notice to this effect is earnestly solicited. The Examiner is invited to phone applicant's attorney if it is believed that a telephonic or personal interview would expedite prosecution of the application.

Respectfully submitted,

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Enclosure: Version With Markings Showing Changes Made

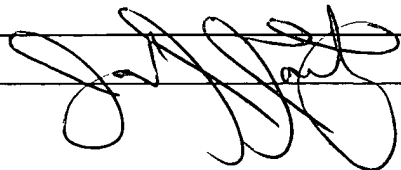
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VERSION WITH MARKINGS SHOWING CHANGES MADE**IN THE CLAIMS:**

Claims 8 and 9 has been cancelled.

Claims 18-21 are newly presented.

Please amend the claims as shown:

5. (Twice Amended) The method for forming a semiconductor device according to claim 16, in which said step f1)[includes] comprises:

depositing said second insulating film using a TEOS-CVD method utilizing TEOS activated by O₃.

9. (Twice Amended) The method for forming a semiconductor device according to claim[8] 16, in which said step f2b [of forming a metal wiring film further includes]comprises heat-treating said TiN layer in a temperature range of 200 to 650°C[after forming said TiN layer].

11. (Twice Amended) The method for forming a semiconductor device according to claim 16,[in which said step f2) includes forming a metal wiring film by: a) depositing a base layer, and b) depositing an Al layer] wherein said upper layer is an Al layer.

12. (Twice Amended) The method for forming a semiconductor device according to claim 11, wherein

said step of depositing[an] said Al layer comprises sputtering while heating said circuit board in a temperature range of 100 to 400°C.

16. (Amended) A method for forming a semiconductor device, comprising the steps of:

- a) providing a circuit board;
- b) forming a first insulating film at least indirectly on said circuit board;
- c) forming a lower electrode on said first insulating film;

- d) forming a ferroelectric film over said lower electrode;
- e) forming an upper electrode over said ferroelectric film, said lower electrode, ferroelectric film, and said upper electrode combining to form a ferroelectric capacitor;
- f) creating a synthetic tensile stress upon said ferroelectric capacitor by:
 - f1) forming a second insulating film over said ferroelectric capacitor;
 - f2) forming a metal wiring[pattern] film over said second insulating film;and
 - f3) forming a surface protective film over said second insulating film and said metal wiring[pattern] film;
 - in which step f2) comprises forming the metal wiring film by:
 - f2a) depositing a TiN layer;
 - f2b) heat-treating said TiN layer to create a tensile stress; and
 - f2c) depositing an upper layer on said TiN layer.

17. (Amended) The method as in claim 16, in which step[f1) includes forming a plurality of contact openings through said second insulating film for contacting said upper electrode and said lower electrode and step f2) includes providing contact between said metal wiring pattern and said upper and lower electrodes through said plurality of contact openings] f2b) comprises heat-treating said TiN layer in a temperature range of 200 to 650°C.